

What is claimed is:

1           1. A clock monitoring apparatus comprising:  
2           a main clock monitoring portion including a first counter  
3           for counting a main clock, issuing a normal operation confirming  
4           flag indicating that a normal operation is being carried out  
5           when the first counter is overflowed or reaches a previously  
6           determined set value, monitoring the normal operation  
7           confirming flag by a sub clock, issuing a first main clock  
8           stop flag having an output in correspondence with H (high level)  
9           / L (low level) of the normal operation confirming flag and  
10          a main clock initializing signal for initializing the main  
11          clock when the main clock is determined to stop and resetting  
12          the first main clock stop flag when the main clock is recovered  
13          by receiving the main clock initializing signal; and  
14          a sub clock switching control portion including a second  
15          counter for counting a signal output produced by calculating  
16          a logical sum of the sub clock and the first main clock stop  
17          flag at fall of the sub clock at a time point of generating  
18          the first main clock stop flag, switching to a sub clock operation  
19          by issuing a sub clock switching signal when the second counter  
20          output is overflowed or reaches a previously determined set  
21          value and resetting the second counter output when the main  
22          clock is recovered and a second main clock stop flag produced  
23          by inverting the first main clock stop flag and delaying the  
24          sub clock by a predetermined period by a main clock monitoring  
25          portion, is reset.

1           2. The clock monitoring apparatus according to Claim  
2 1, wherein the second main clock stop flag generating portion  
3 outputs the main clock initializing signal by calculating a  
4 logical sum of the first main clock stop flag and the second  
5 main clock stop flag.

1           3. The clock monitoring apparatus according to Claim  
2 2, further comprising:

3           a first logical product circuit for calculating a logical  
4 product of a main clock temporarily stopping signal for  
5 temporarily stopping the main clock and an output signal from  
6 the first logical sum circuit; and

7           a second logical product circuit for calculating a  
8 logical product of the main clock temporarily stop signal and  
9 an output signal from the second counter.

1           4. The clock monitoring apparatus according to Claim  
2 1, wherein the main clock monitoring portion comprising:

3           a main clock monitoring circuit for counting the main  
4 clock by the first counter, issuing the normal operation  
5 confirming flag when the first counter is equal to the  
6 predetermined set value or overflowed and monitoring the normal  
7 operation confirming flag at fall of the sub clock;

8           a first main clock stop flag generating portion for  
9 issuing the first main clock stop flag constituting "H" when  
10 the normal operation confirming flag is "H" and constituting

11 "L" when the normal operation confirming flag is "L" at fall  
12 of the sub clock; and  
13 a second main clock stop flag generating portion for  
14 issuing the second main clock stop flag and the main clock  
15 initializing signal when the main clock is stopped.

1 5. The clock monitoring apparatus according to Claim  
2 1, wherein when the main clock is recovered by receiving the  
3 main clock initializing signal, the main clock monitoring  
4 portion resets the second main clock stop flag.

1 6. The clock monitoring apparatus according to Claim  
2 1, wherein the sub clock switching control portion includes  
3 a second logical sum circuit for calculating a logical sum  
4 of the first main clock stop flag and the sub clock, making  
5 the second counter count the logical sum signal at a time point  
6 of generating the main clock stop flag, switching to the sub  
7 clock operation by issuing the sub clock switching signal when  
8 the second counter is overflowed or reaches the set value and  
9 returning to a standby state by resetting the second counter  
10 when the main clock is recovered and the main clock stop flag  
11 is reset.

1 7. The clock monitoring apparatus according to Claim  
2 6, wherein in a case in which the main clock stays to be stopped  
3 even when the main clock is stopped and the main microcomputer  
4 is initialized, the second counter is overflowed and a sub

5 clock switching signal is issued by the sub clock switching  
6 control portion.

1 8. The clock monitoring apparatus according to Claim  
2 1, further comprising:

3 a sub clock self monitoring portion capable of issuing  
4 an all clock stop flag indicating that all the clocks are stopped  
5 when the sub clock is stopped, initializing automatically the  
6 main clock when the main clock is stopped and carrying out  
7 a continuing operation under a state before abnormality when  
8 the main clock is recovered thereby.

1 9. The clock monitoring apparatus according to Claim  
2 8:

3 wherein the sub clock self monitoring portion comprising:  
4 a first delaying adding circuit for issuing a first delay  
5 signal for delaying the sub clock by a predetermined period  
6 and a second delay adding circuit for issuing a second delay  
7 signal for delaying the first delay signal by the predetermined  
8 period;

9 an exclusive-OR circuit for calculating an exclusive-OR  
10 of the sub clock, the first delay signal and the second delay  
11 signal; and

12 a third logical product circuit for calculating a logical  
13 product of the second main clock stop flag and an inverted  
14 signal of a signal produced by calculating the exclusive-OR;

15 wherein an all clock stop flag is outputted from the

16 third logical product circuit.

1 10. The clock monitoring apparatus according to Claim  
2 9, further comprising:

3 a first logical product circuit for calculating a logical  
4 product of a main clock temporarily stopping signal for  
5 temporarily stopping the main clock and an output signal from  
6 the first logical sum circuit;

7 a second logical product circuit for calculating a  
8 logical product of the main clock temporarily stopping signal  
9 and an output signal from the second counter; and

10 a third logical product circuit for calculating a logical  
11 product of the main clock temporarily stopping signal and an  
12 output signal from the third logical sum circuit.